A Single-Stage Primary-Side-Controlled Off-line Flyback LED Driver With Ripple Cancellation

Peng Fang, *Student Member, IEEE*, Ya-jie Qiu, *Student Member, IEEE*, Hongliang Wang, *Senior Member, IEEE*, and Yan-Fei Liu, *Fellow, IEEE*

***Abstract*—Ripple cancellation LED driver can achieve flicker-free LED driving while maintaining high power factor, high efficiency, and low component cost. It is a very competitive solution compared to a conventional single-stage or two-stage LED driver design. In this paper, a primary-side-controlled ripple cancellation LED driver has been proposed. The voltages of the proposed LED driver are sensed at the primary side by transformer sensing windings. The LED current is also obtained by sensing the primary-side switching current. The entire control circuit is built on the primary side. All the advantages from the existing ripple cancellation LED drivers are maintained while achieving the primary-side control. Based on the proposed circuit, a potential integrated primary-side controller can be designed, which can significantly reduce the component cost and design complexity. A 30-W, 50-V, 0.6-A experimental prototype with a universal input voltage range has been built to verify the proposed LED driver.**

***Index Terms*—Flicker-free LED driving, high power factor, primary side control, ripple cancellation.**

I. Introduction

LED lighting becomes increasingly popular because of high efficacy, low power consumption, and long life span compared to the conventional alternatives. Usually, a specially designed power supply—LED driver—is needed to regulate the current in the LEDs. A single-stage LED driver is a desirable choice for achieving low cost and high efficiency. Fig. 1 illustrates a conventional single-stage flyback LED driver and its typical output waveforms.

However, when a high power factor is achieved with a single-stage off-line LED driver, an energy imbalance presents between the input side and the output side [1], regardless of which topologies or controlling methods are used. The energy imbalance creates a significant twice-line-frequency voltage ripple across LED, which causes an even larger twice-line-frequency ripple LED current. The twice-line-frequency ripple LED current is manifested as the so-called twice-line-frequency lighting flicker through LEDs. The excessive flicker can lead to various human health-related issues [2], [3]. In this paper, the ripple at twice-line-frequency is of particular interest. In the following, the term "ripple" mean twice-line-frequency ripple, unless stated otherwise.

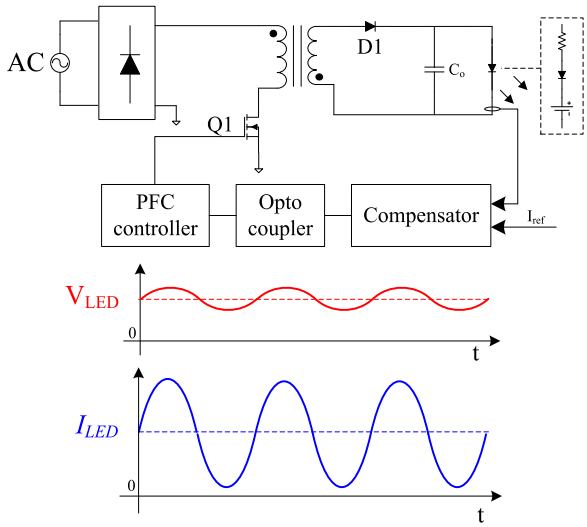

Fig. 1. Conventional flyback LED driver and its typical waveform.

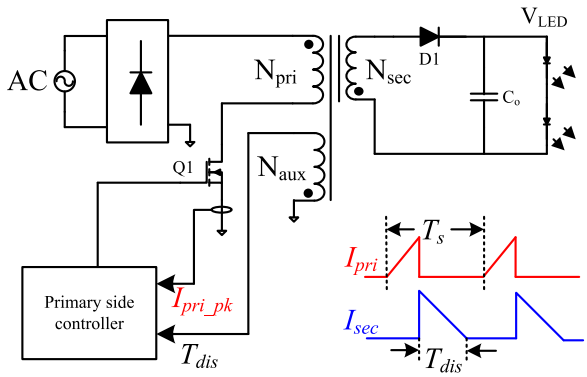

Fig. 2. Primary-side-controlled LED driver.

Among many popular single-stage LED driver designs, the flyback LED driver is a very attractive LED driving solution for isolated applications. The primary-side controlled technology [4]–[7] makes the flyback LED driving solution even more cost effective. The concept of the primary-side controlled flyback LED driver is illustrated in Fig. 2.

The peak switching current of the primary-side winding $I_{\mathrm{pri\_pk}}$ is sensed. With the coupling relationship between the

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The authors are with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3N6, Canada (e-mail: p.fang@queensu.ca; yajie.qiu@queensu.ca; hongliang.wang@queensu.ca; yanfei.liu@queensu.ca).

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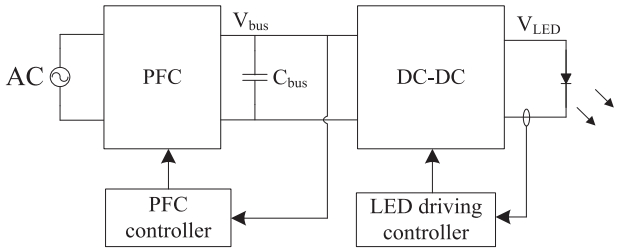


Fig. 3. Two-stage LED driver implementation.

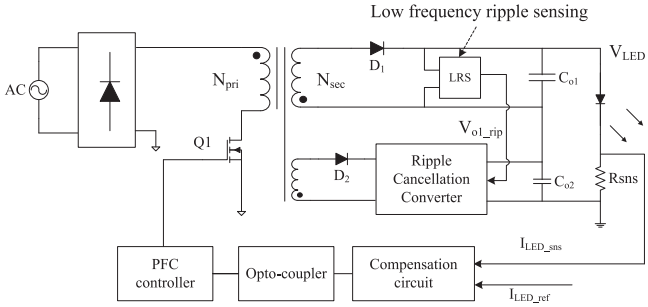


Fig. 4. Flyback implementation of the ripple cancellation LED driver.

primary-side winding $N_{\rm pri}$ and the secondary-side winding $N_{\rm sec}$, the peak secondary-side switching current is essentially sensed. The magnetic current in the secondary-side winding is discharged after the MOSFET Q_1 is turned off. The moment that the secondary-side current becomes zero is detected by sensing the voltage change on the transformer windings. Therefore, the secondary-side current discharge time $T_{\rm dis}$ is obtained. With $I_{\rm pri\_pk}$ and the discharge time $T_{\rm dis}$ being available, the averaged secondary-side current in a switching cycle can be obtained, which is also equal to the LED current. Therefore, only one controller is needed at the primary side to regulate the LED current. No secondary-side compensation circuit and no opto-coupler are needed, as shown in Fig. 1. This way, the component cost and design complexity are further reduced. However, the conventional primary-side control LED driver did not include any measures to solve the flicker issues.

A two-stage LED driver [8], [9] can naturally achieve flicker-free LED driving and maintains a high power factor. Fig. 3 illustrates a two-stage LED driver structure. The first PFC stage achieves a high power factor for the entire system, while the second-stage dc–dc converter filters out the twice-line-frequency ripple on the output voltage of the first stage and produces a dc LED voltage to drive LEDs. However, the drawback of a two-stage LED driver is also very obvious. The power delivered to the output has been processed twice in a two-stage design, which significantly reduces the efficiency as compared to a single-stage design. The power component and the control circuit are also much more expensive in a two-stage design.

A lot of research has been done with the attempt to combine the advantages from the single-stage and the two-stage design. There are a variety of integrated solution [10]–[15] combine the front-end PFC and the second stage dc-dc. Integrated boost half-bridge LED driver [10]–[12], integrated buck–flyback LED driver [13], integrated SEPIC–flyback LED driver [14] and integrated SEPIC Class-E LED driver [15] have been proposed. In these schemes, the power components are shared between the front-end PFC and the second-stage dc–dc converter. They achieved a reduced component count as compared to a standard two-stage LED driver. However, the ac input power is still converted two times with these topologies. Also, these designs are complicated and have a lot of restrictions to perform both power factor correction and dc–dc conversion simultaneously with shared power components. The PFC and the second-stage dc–dc cannot work at the optimum condition at the same time and the voltage stress and/or current stress of the shared switches are usually increased. The method of active energy storage LED driving [16], [17] was also proposed. A bidirectional dc–dc converter works as an active energy storage device to buffer the energy difference between the input and output. Flicker-free LED driving can be achieved with this method. However, roughly one-third of the total output power (the power difference between the input and the output in a half line cycle) is converted back and forth (two times) by the bidirectional dc–dc converter, which introduces significant power loss. The complicated control scheme and high component cost with the bidirectional dc–dc converter make this solution less desirable. The method of injecting harmonics input current [18], [19] was proposed. The LED ripple current is reduced at the expense of reducing power factor. This method can reduce the level of flicker but cannot completely remove it.

The ripple cancellation LED driving technologies [20]–[26] have been proposed, and a general implementation of the isolated ripple cancellation LED driver is illustrated in Fig. 4. A ripple cancellation converter (RCC) is located at the secondary-side and produces an opposite low-frequency ripple voltage to cancel the ripple voltage from the PFC. This way, a pure dc LED voltage is produced and is applied to the LED load to generate a dc LED current. Because the RCC only provides an opposite ripple voltage for cancellation while delivering a small amount of power, the efficiency of the complete LED driver with RCC is close to the efficiency of a comparable single-stage LED driver. The implementation cost of the RCC is also much lower as compared to the second-stage dc–dc converter in a comparable two-stage design. However, there is still space to further reduce the component cost.

With the present RCC technology, as shown in Fig. 4, two control loops are required. A voltage loop is used to regulate the RCC output to generate an out of phase ripple voltage and a current loop is used to regulate the LED current. The control circuit is populated at both the primary side and at the secondary side.

A primary-side-controlled ripple cancellation LED driver has been proposed in [27] to further reduce the implementation cost of the ripple cancellation LED driver. The new method maintains the advantages of the ripple cancellation LED driver and provides a significant improvement—primary-side control. A control circuit is designed specifically to enable the implementation of the proposed ripple cancellation power topology and achieve primary-side control. No secondary-side control circuit is needed, and the opto-coupler can also be eliminated. This paper is a significantly improved version of the conference paper with more detailed analysis and more clear design guideline.

This paper is organized as follows. Section II describes the structure of the proposed LED driver. Section III analyzes the power stage design of the proposed LED driver. Section IV discusses the detailed primary-side control structure of the proposed LED driver. The experimental result is presented in Section V, and the paper is concluded in Section VI.

II. Structure of the Proposed LED Driver

In this section, the structure of the proposed primary-side-controlled ripple cancellation LED driver is discussed.

Fig. 5 shows the structure of the proposed LED driver. The power stage includes a main PFC flyback (on the top) and a miniature flyback (on the bottom) converter that serves as the RCC. The PFC flyback is connected with the rectified ac source to achieve a high power factor for the system. The input of the RCC flyback is from an auxiliary output voltage of the PFC flyback located at the primary side. The RCC flyback is used to produce an opposite ripple voltage $V_{\rm o2}$ to compensate the twice-line-frequency ripple voltage from the PFC flyback output $V_{\rm o1}$. Under this power stage structure, a dc LED voltage is produced and is used to drive the LED load with a dc current - flicker-free LED driving. It is noted that the design of some practical circuitry, such as the EMI filter and the snubber circuit are not different from that of the other conventional designs. They are not shown in Fig. 5 in order to keep the discussion concise.

Another good feature of the proposed LED driver is the proposed primary-side control system. A conventional primary-side LED driving controller cannot be used with the proposed power topology. A new primary-side controller circuit is also presented in this paper to work with the proposed power topology. The output voltage of the PFC flyback $V_{\rm o1}$ is sensed by the sensing winding $N_{\rm sns1}$ and the output voltage of the RCC flyback $V_{\rm o2}$ is sensed by the sensing winding $N_{\rm sns2}$. Current sensing is performed at the primary side of the RCC flyback. The peak switching current $I_{\rm pk\_sns}$ and the zero-current condition (ZCS) of the secondary-side current are sensed. The basic operating principle of the current sensing circuit in the proposed LED driver is the same as the popular off-the-shelf controllers, such as FL7732, IRS2983, and RT7304. The difference with ours is we need to take the proposed power topology into consideration. To be precise, the current sensing needs to be performed on the primary side of the RCC flyback instead of the primary side of the PFC flyback. The reason of this circuit arrangement will be explained in Section IV. Therefore, the entire control system is located on the primary side. No secondary-side compensation circuit and opto-coupler are needed.

Fig. 6 reveals the detailed working mechanism of the proposed primary-side controller. There are four inputs for the controller: $V_{\rm o1\_sns}$, $V_{\rm o2\_sns}$, $I_{\rm pk\_sns}$, and ZCS. There are two control loops in the system, the voltage loop to regulate the RCC flyback output $V_{\rm o2}$ and the current loop to regulate the LED current. In order to control the RCC flyback output $V_{\rm o2}$ with an opposite ripple voltage to that of the PFC flyback output $V_{\rm o1}$, the output voltage $V_{\rm o1}$ is sensed by the sensing winding $N_{\rm sns1}$. $V_{\rm o1\_sns}$ is the voltage across the sensing winding $N_{\rm sns1}$. The voltage on the sensing winding is sampled at the right timing by the S & H circuit. This way, the PFC flyback output voltage $V_{\rm o1}$ is replicated at the primary side. The replicated PFC flyback output voltage $V_{\rm o1\_replica}$ is then level shifted and inverted and becomes the reference voltage $V_{\rm o2\_ref}$ for the RCC flyback output. Likewise, the RCC flyback output is also sensed at the primary side. With a well-designed control loop, the RCC flyback output will tightly follow its reference. An opposite twice-line-frequency ripple voltage is produced to compensate the ripple voltage from the PFC flyback output. The primary-side current sensing is a part of the control scheme. The signal $I_{\rm pk\_sns}$ represents the primary-side peak switching current of the RCC flyback transformer. The signal ZCS is the detection signal when the secondary-side switching current of the RCC flyback transformer reaches zero. With known $I_{\rm pk\_sns}$ and ZCS, the LED current can be calculated at the primary side. The calculated LED current follows the current reference so that the LED current is regulated. The PFC controller is in the LED current regulation loop. It will automatically adjust the dc voltage of the PFC flyback output to regulate LED current.

III. Detailed Analysis on the Power Stage

In Section III, the design consideration for the power stage of the proposed primary-side-controlled ripple cancellation LED driver is discussed.

A. PFC Flyback Design

From Fig. 5, the PFC flyback has two outputs, $V_{\rm o1}$ and $V_{\rm aux}$. Because the majority of the power delivered to the LED load is through output $V_{\rm o1}$, $C_{\rm o1}$ serves as the storage capacitor to buffer the energy difference between the input and the output in a half line cycle. The energy difference is presented as the twice-line-frequency ripple voltage on $V_{\rm o1}$. The ripple is almost reversely proportional to the capacitance of $C_{\rm o1}$. Their relationship can be expressed approximately as

$$C_{o1} \approx \frac{I_{\rm LED}}{2 \times \pi \times f_{\rm line} \times V_{o1\_{\rm rip\_pp}}}. \tag{1}$$

In (1), $V_{\rm o1\_rip\_pp}$ is the peak-to-peak amplitude of the twice-line-frequency ripple voltage of $V_{\rm o1}$. Therefore, when a smaller capacitor C_{o1} is used, the ripple voltage on $V_{\rm o1}$ will be larger. This is a major concern for a conventional high-power-factor single-stage flyback LED driver. The ripple voltage is strictly limited to avoid severe flicker. Because the ripple voltage from the PFC flyback is compensated by the ripple from the RCC flyback output, a dc alike LED voltage and LED current can be produced. Therefore, a relatively larger ripple voltage from the PFC flyback output V_{o1} is acceptable in the design. This significantly reduces the amount of capacitance required for C_{o1}. Fig. 7 plots the relationship between the peak-to-peak ripple voltage of the PFC flyback output V_{o1} and the capacitance of C_{o1}. For example, when the peak-to-peak twice-line-frequency ripple voltage is limited to 1 V, the required output capacitor is around 1600 μF. On the other hand, when the peak-to-peak twice-line-frequency ripple voltage is allowed to be as large as 10 V, the required output capacitor is reduced to only 160 μF. It is also found that when the peak-to-peak ripple voltage is beyond 7 V, the reduction on the output capacitor becomes insignificant. Taking the advantage of ripple cancellation, C_{o1} can be

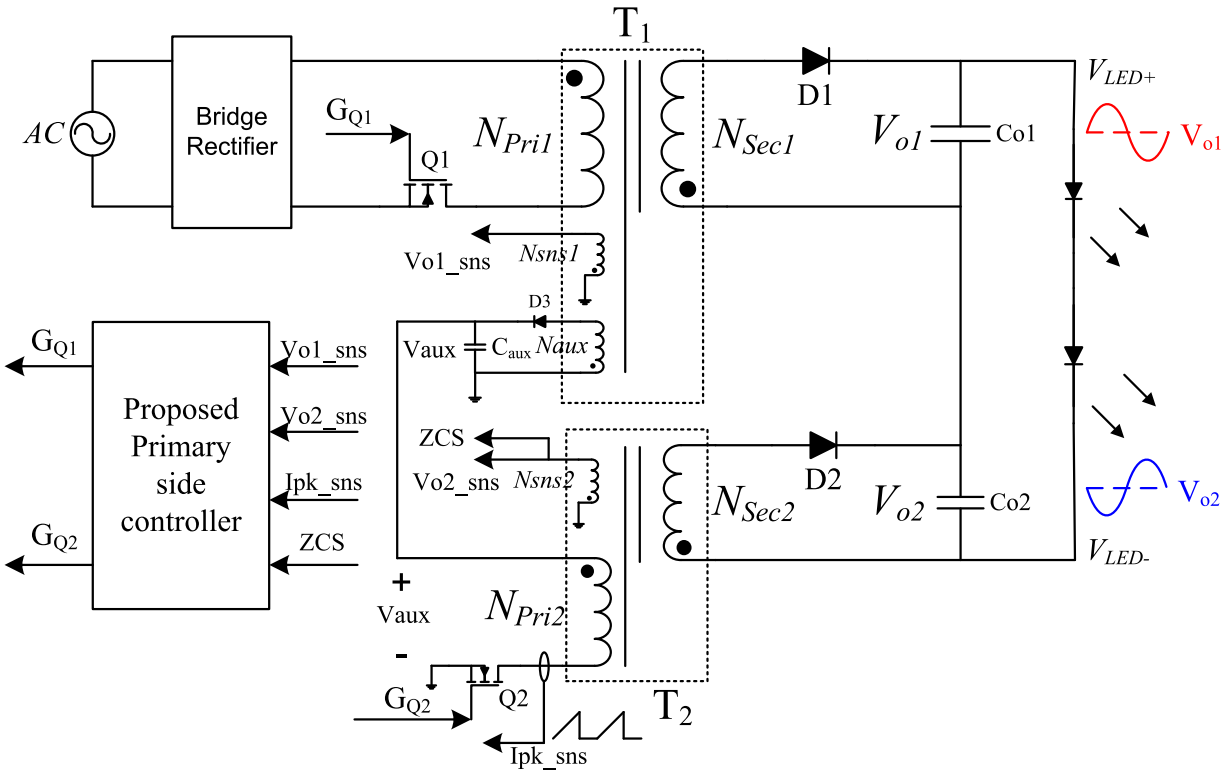


Fig. 5. Structure of the proposed primary-side-controlled ripple cancellation LED driver.

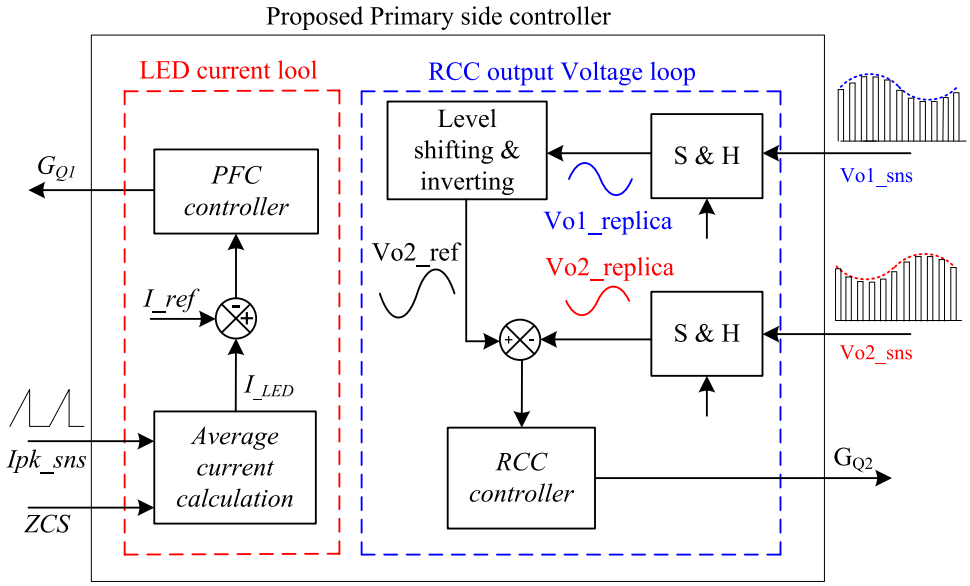


Fig. 6. Diagram of the proposed primary-side controller (all the terminal voltages are shown in Fig. 5).

selected much smaller in the proposed primary-side-controlled ripple cancellation LED driver than it is in a conventional design, which significantly reduces the cost.

However, the amplitude of the ripple voltage has an impact on the overall efficiency. Referring to Fig. 5, the input voltage of the RCC flyback $V_{\rm aux}$ is produced by the PFC flyback at the primary side. Therefore, the power delivered to the LED load through the RCC flyback has been processed twice. It is desirable to reduce the power delivered by the RCC flyback. This means the dc output voltage of V_{o2} should be designed as small as possible. Fig. 8 illustrates two cases of different peak-to-peak ripple amplitude of the PFC flyback output. When a higher ripple voltage is presented on the PFC flyback output, a higher dc output is needed from the RCC flyback to provide bias voltage for the twice-line-frequency ripple.

As a guideline, the dc voltage of the RCC flyback output can be designed to be no more than 10% of the overall LED voltage. For example, the averaged V_{o2} is less than 5 V, while the LED

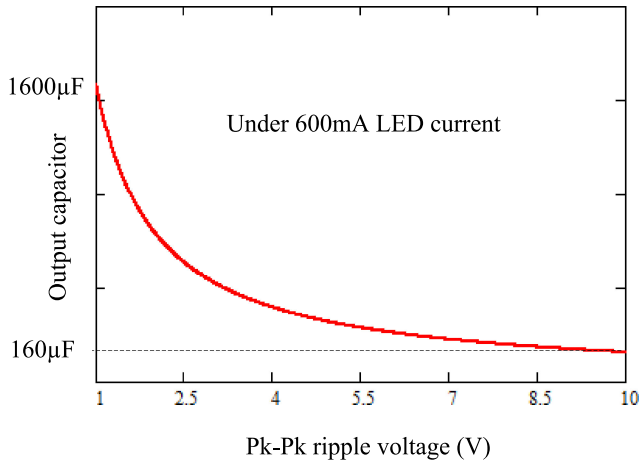


Fig. 7. Relationship between the peak-to-peak ripple voltage on V_{o1} and the required output capacitor C_{o1}.

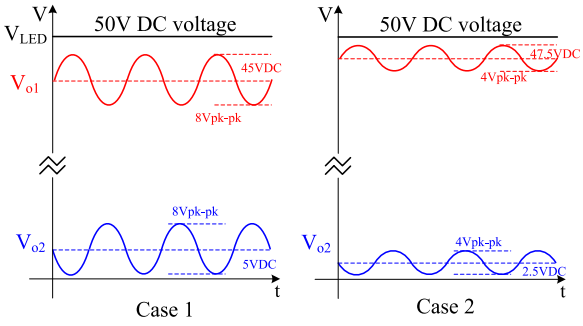


Fig. 8. Comparison of two cases to illustrate the relationship between the PFC flyback ripple voltage and the overall efficiency.

voltage is 50 V. This also indicates that the peak-to-peak twice-line-frequency ripple voltage should be lower than 10 V so that the RCC flyback output voltage is always above zero. Under this condition, the power delivered by the RCC flyback only contributes less than 10% of the total output power, and the overall efficiency of the proposed LED driver should be close to a conventional single-stage LED driver.

The overall efficiency of the proposed LED driver can be expressed as

$$\eta_{\mathrm{LED\_dr}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{P_{\mathrm{PFC}} + P_{\mathrm{RCC}}}{(P_{\mathrm{PFC}}/\eta_{\mathrm{PFC}}) + (P_{\mathrm{RCC}}/(\eta_{\mathrm{PFC}} \times \eta_{\mathrm{RCC}}))}. \quad (2)$$

In (2), $P_{\mathrm{in}}, P_{\mathrm{out}}, P_{\mathrm{PFC}},$ and $\mathrm{P_{RCC}}$ are the input power, the total output power, the PFC flyback output power, and the RCC output power, respectively. η_{PFC} and η_{RCC} are the efficiencies of the PFC flyback and the RCC flyback, respectively. For example, if the RCC flyback delivers 10% of the output power and both the PFC flyback and the RCC Flyback achieve 88% efficiency, the overall efficiency is calculated to be 86.8%, which is only 1.2% lower than the PFC flyback. In order to achieve the same efficiency with a two-stage LED driver, the second dc–dc converter needs to achieve 0.868/ 0.88 = 98.6% efficiency, which is difficult. The advantageous power stage structure of the proposed LED driver enables an overall high-efficiency design.

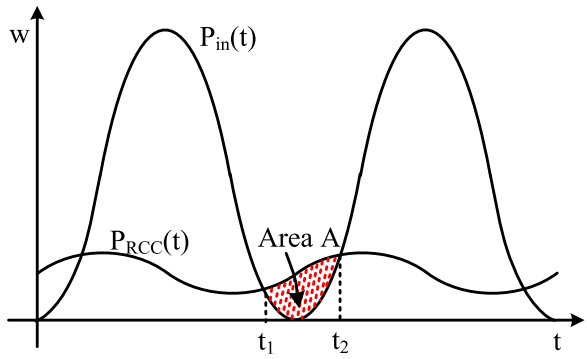


Fig. 9. Plot of the input power and RCC flyback output power.

As referring to Fig. 5, C_{aux} is the output capacitor of V_{aux} and also serves as the input capacitor of the RCC flyback. When the instantaneous input power is higher than the instantaneous output power of the RCC flyback, C_{aux} serves as a high-frequency filter capacitor. It also act as the reservoir capacitor that provides energy to sustain the RCC flyback when the input power is not enough. It is noted that majority energy is stored in C_{o1}.

Fig. 9 plots the waveform of the ac input power and the output power of the RCC flyback. During the time interval $[t_1 - t_2]$, the instantaneous input power is close to zero and is lower than the power required sustaining the RCC flyback. The capacitor C_{aux} supplies the difference to maintain the RCC flyback. Therefore, C_{aux} should be selected to ensure that its voltage during $[t_1 - t_2]$ is within the expected range.

In Fig. 9, area A represents the energy difference between the input power and the RCC flyback output power during $[t_1 - t_2]$. Area A can be expressed as

$$\mathrm{Area}_A = \int_{t_1}^{t_2} p_{\mathrm{RCC}}(t)dt - \int_{t_1}^{t_2} p_{\mathrm{in}}(t)dt \quad (3)$$

where

$$P_{\mathrm{in}} = V_{\mathrm{in\_rms}} \times I_{\mathrm{in\_rms}} + V_{\mathrm{in\_rms}} \times I_{\mathrm{in\_rms}} \cos(4\pi \times f_{\mathrm{line}} \times t) \quad (4)$$

$$P_{\mathrm{RCC}}(t) = V_{\mathrm{o2\_dc}} \times I_{\mathrm{LED}} + \frac{1}{2} V_{\mathrm{o2\_rip\_pp}} \times I_{\mathrm{LED}} \times \cos(4\pi \times f_{\mathrm{line}} \times t + \Phi). \quad (5)$$

In (5), $V_{\mathrm{o2\_dc}}$ and $V_{\mathrm{o2\_rip\_pp}}$ are the dc voltage and the peak-to-peak ripple of V_{o2}, respectively. Φ is the phase difference between the ripple of the input power and the ripple of the voltage V_{o2}. Approximately, Φ is equal to $3\pi/2$.

In order to simplify the calculation, it is assumed that all the energy to sustain RCC flyback operation is provided by C_{aux} during $[t_1 - t_2]$. Therefore, area A can be approximately expressed as

$$\mathrm{Area}_A \approx \int_{t_1}^{t_2} p_{\mathrm{RCC}}(t)dt. \quad (6)$$

With closely inspecting the waveforms $P_{\rm in}(t)$ and $P_{\rm RCC}(t)$, it can also found that $P_{\rm RCC}(t)$ is in the vicinity of its averaged value during $[t_1 - t_2]$. Therefore, (6) can be further simplified approximately as

$$\text{Area}_A \approx p_{\rm RCC\_avg} \times (t_2 - t_1). \tag{7}$$

It can also assume that the value of the crossover points between $P_{\rm in}(t)$ and $P_{\rm RCC}(t)$ at time t_1 and t_2 are equal to $P_{\rm RCC\_avg}$. Therefore, the angular difference $\theta_{t_1-t_2}$ between t_1 and t_2 can be approximately expressed as

$$\theta_{t_1-t_2} = 2 \times \arccos\left[1 - \frac{P_{\rm RCC\_avg}}{P_{\rm LED}}\right]. \tag{8}$$

The time $t_2 - t_1$ can be expressed as

$$t_2 - t_1 = \frac{\arccos\left[1 - \frac{P_{\rm RCC\_avg}}{P_{\rm LED}}\right]}{\pi \times f_{\rm line}}. \tag{9}$$

Substituting (9) into (7) yields

$$\text{Area}_A \approx p_{\rm RCC\_avg} \times \frac{\arccos\left[1 - \frac{P_{\rm RCC\_avg}}{P_{\rm LED}}\right]}{\pi \times f_{\rm line}}. \tag{10}$$

In (9) and (10), $P_{\rm LED}$ represents the total output LED power. On the other hand, the energy provided by $C_{\rm aux}$ causes a voltage drop $\Delta V_{\rm aux}$ on $V_{\rm aux}$. The relationship between the area *A* and the voltage drop on $V_{\rm aux}$ can be expressed as

$$\text{Area}_A = \frac{1}{2} C_{\rm aux}(2V_{\rm aux} + \Delta V_{\rm aux})\Delta V_{\rm aux}. \tag{11}$$

In (11), $\Delta V_{\rm aux}$ represents the voltage drop during the time interval $[t_1 - t_2]$. Assuming that the voltage drop $\Delta V_{\rm aux}$ is equal to $k \cdot V_{\rm aux}$ in the design, (11) can be rewritten as

$$\text{Area}_A = \frac{1}{2} C_{\rm aux} \times (2 + k) \times V_{\rm aux} \times k \times V_{\rm aux}. \tag{12}$$

Comparing (10) and (12) yields

$$C_{\rm aux} \approx \frac{2 \times P_{\rm RCC\_avg} \times \arccos\left[1 - \frac{P_{\rm RCC\_avg}}{P_{\rm LED}}\right]}{{V_{\rm aux}}^2 \times (2 + k) \times k \times \pi \times f_{\rm line}}. \tag{13}$$

In a given design, based on the predefined $V_{\rm aux}$, $P_{\rm RCC\_avg}$ and the constant *k*, capacitor $C_{\rm aux}$ can be calculated based on (13). For example, with $V_{\rm aux}$ to be 15 V, $P_{\rm RCC\_avg}$ to be 3 W, and the coefficient *k* to be 0.2, the required $C_{\rm aux}$ is calculated to be $\sim$144 μF. $C_{\rm aux}$ can be implemented with electrolytic capacitors to save cost. With properly selecting the ripple current rating of the capacitor, the life span of $C_{\rm aux}$ can be as long as the PFC flyback output electrolytic capacitor, and it will not become the limiting factor of the life span of the LED driver.

B. RCC Flyback Design

In order to adopt the primary-side current sensing method with the proposed LED driver, the flyback RCC needs to operate under boundary conduction mode (BCM) or discontinuous conduction mode (DCM). In any switching cycle, the averaged secondary-side current is equal to the LED current plus the current charging/discarding the RCC flyback output capacitor. Therefore

$$\frac{I_{\rm sec\_pk2} \times T_{\rm dis}}{2 \times T_s} = I_{\rm LED} + C_{o2} \times \frac{dV_{o2}}{dt}. \tag{14}$$

In (14), $T_{\rm dis}$ represents the magnetic current discharge time and T_s represents a switching period. The term $C \times \frac{dV_{o2}}{dt}$ represents the charging/discharging current of the RCC flyback output capacitor C_{o2} in one switching cycle. Since the capacitor C_{o2} is used to filter the high-frequency ripple voltage and is in the magnitude of a few microfarads, the term $C \times \frac{dV_{o2}}{dt}$ is much smaller than $I_{\rm LED}$ and can be ignored in the calculation.

Also, the peak secondary-side current can be expressed as

$$I_{\rm sec\_pk2} = I_{\rm pri\_pk2} \times \frac{N_{\rm pri2}}{N_{\rm sec\,2}}. \tag{15}$$

Combining (14) and (15) yields

$$\frac{I_{\rm pri\_pk2} \times T_{\rm dis}}{2 \times T_s} \times \frac{N_{\rm pri2}}{N_{\rm sec\,2}} = I_{\rm LED}. \tag{16}$$

The peak primary-side current can be also expressed as

$$I_{\rm pri\_pk2} = \frac{V_{\rm in} \times T_{\rm on}}{L_{\rm pri2}}. \tag{17}$$

Combining (16) and (17) yields

$$\frac{V_{\rm in} \times T_{\rm on} \times T_{\rm dis}}{2 \times T_s \times L_{\rm pri2}} \times \frac{N_{\rm pri2}}{N_{\rm sec\,2}} = I_{\rm LED}. \tag{18}$$

Because the flyback RCC works either under DCM or BCM condition, a voltage-second balance is achieved in every switching cycle. Therefore

$$V_{\rm in} \times T_{\rm on} \times \left(\frac{N_{\rm sec\,2}}{N_{\rm pri2}}\right) = V_{o2} \times T_{\rm dis}. \tag{19}$$

In (19), $T_{\rm on}$ is the turn on time of the MOSFET Q_2 (the main MOSFET of the RCC flyback) and $T_{\rm dis}$ is the magnetic current discharge time during turn off. Equation (19) can be further rearranged as

$$T_{\rm dis} = \frac{V_{\rm in} \times T_{\rm on} \times (N_{\rm sec\,2}/N_{\rm pri2})}{V_{o2}}. \tag{20}$$

Substituting (20) into (18) yields

$$I_{\rm LED} = \frac{(V_{\rm in} \times T_{\rm on})^2}{2 \times T_s \times L_{\rm pri2} \times V_{o2}}. \tag{21}$$

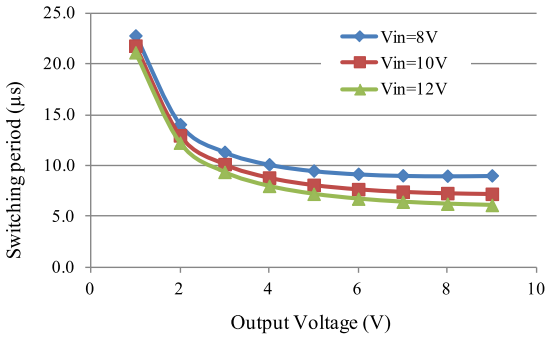
Rearranging (21) yields

$$T_{\rm on} = \frac{\sqrt{2 \times I_{\rm LED} \times T_s \times L_{\rm pri2} \times V_{o2}}}{V_{\rm in}}. \tag{22}$$

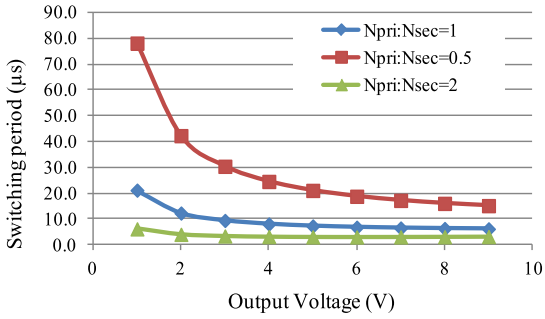
Substituting (22) into (20) yields

$$T_{\rm dis} = \frac{\sqrt{2 \times I_{\rm LED} \times T_s \times L_{\rm pri2} \times V_{o2}}}{V_{o2}} \times \frac{N_{\rm sec\,2}}{N_{\rm pri2}}. \tag{23}$$

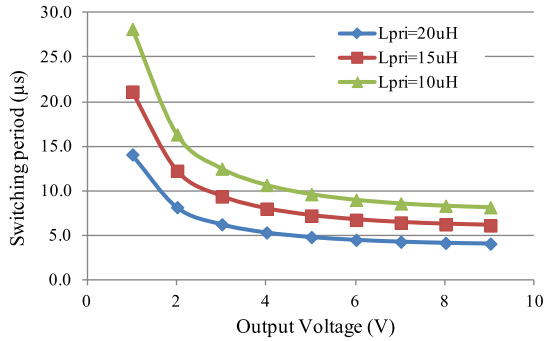
When the flyback RCC works under BCM mode, $T_{\rm dis}$ is equal to the turn off time, ignoring the practical delay between the magnetic current drops to zero and the starting of the next



(a)



(b)



(c)

Fig. 10. Relationship between T_s and the RCC flyback output voltage V_{o2}: (a) Under $N_{\mathrm{pri2}}{:}N_{\mathrm{sec2}} = 1, L_{\mathrm{pri2}} = 15\ \mu\mathrm{H}, \mathrm{I}_{\mathrm{LED}} = 0.6$ A. (b) Under $V_{\mathrm{in}} = 12$ V, $L_{\mathrm{pri2}} = 15\,\mu\mathrm{H}, \mathrm{I}_{\mathrm{LED}} = 0.6$ A. (c) Under $V_{\mathrm{in}} = 12$V, $N_{\mathrm{pri2}} : N_{\mathrm{sec2}} = 1, I_{\mathrm{LED}} = 0.6$ A.

switching cycle. Therefore

$$T_s = T_{\mathrm{on}} + T_{\mathrm{dis}} = \sqrt{2 \times I_{\mathrm{LED}} \times T_s \times L_{\mathrm{pri2}} \times V_{o2}} \left(\frac{1}{V_{\mathrm{in}}} + \frac{N_{\mathrm{sec2}}}{N_{\mathrm{pri2}} \times V_{o2}} \right). \tag{24}$$

Rearranging (24) yields

$$T_s = 2 \times I_{\mathrm{LED}} \times L_{\mathrm{pri2}} \times V_{o2} \times \left(\frac{1}{V_{\mathrm{in}}} + \frac{N_{\mathrm{sec2}}}{N_{\mathrm{pri2}} \times V_{o2}} \right)^2 \tag{25}$$

Equation (25) shows that T_s changes with $I_{\mathrm{LED}}, L_{\mathrm{pri2}}$, V_{in}, V_{o2}, and the turn's ratio $N_{\mathrm{sec2}}/\mathrm{N}_{\mathrm{pri2}}$. The switching period under different design parameters is plotted in Fig. 10.

The *X*-axis represents the output voltage of the RCC flyback, while the *Y*-axis represents the switching period T_s. For example, with the green curve ($V_{\mathrm{in}} = 12$ V) in Fig. 10(a), the switching period changes from 21 to 6 μs with the change in the output voltage from 1 to 9 V. By choosing the output voltage range, the switching period/frequency can be controlled within a predefined range. Also, other design parameters, such as the turn's ratio $N_{\mathrm{pri2}}{:}N_{\mathrm{sec2}}$, the primary-side inductance L_{pri}, and the input voltage can also change the switching period of the flyback RCC. One should make sure that the BCM controller can properly operate in the whole operation range. If a constant switching frequency controller is used to build the flyback RCC, one should make sure that the switching period of the controller is greater than the sum of T_{on} and T_{off} under the entire operation condition.

IV. Detailed Analysis of the Proposed Primary-Side Controller

As shown in Fig. 5, the output voltage of the PFC flyback and the RCC flyback are sensed by the sensing windings. As also shown in Fig. 6, the signals from the sensing windings are further sampled and conditioned to achieve RCC flyback output regulation. The switching current of the RCC flyback is also sensed at the primary side to achieve LED current regulation. In this section, the voltage and current sense scheme is discussed in more details.

A. Existing Primary-Side Voltage Sensing

Fig. 11 shows the primary-side voltage sensing circuit and the critical waveforms based on the flyback topology. The impact of the output diode's forward voltage drop, parasitic components of the power circuit, and the sampling timing were analyzed in previous literature [28]–[31] and will not be repeated in this paper. A brief introduction of the technology is given as a preparation for better understands the special treatment used to sense the PFC flyback output voltage.

During the turn off period while the output diode D_1 is still conducting, the winding voltage V_{sec} is clamped at the output voltage V_o, ignoring the diode D_1's forward voltage drop and other parasitic circuit parameters. The voltage on winding N_{sec} is proportionally coupled to winding N_{sns}. The voltage on the sensing winding is sampled and held until the next sampling action. In order to avoid excessive voltage ringing on the sensing winding, the sample action should be delayed after turning off the primary-side MOSFET Q_1. Thus, the secondary-side output voltage V_o is obtained at the primary-side cycle by cycle and is presented as V_{o_replica}.

B. Modified Primary-Side Voltage Sensing Method for PFC Flyback

The previous primary-side voltage sensing technology is applied in the context of dc–dc converter. When this voltage sensing method is used to sense the PFC flyback output, the voltage on the sensing winding is not valid during the input voltage zero-crossing. This problem is discussed in details, and a solution is provided in this section.

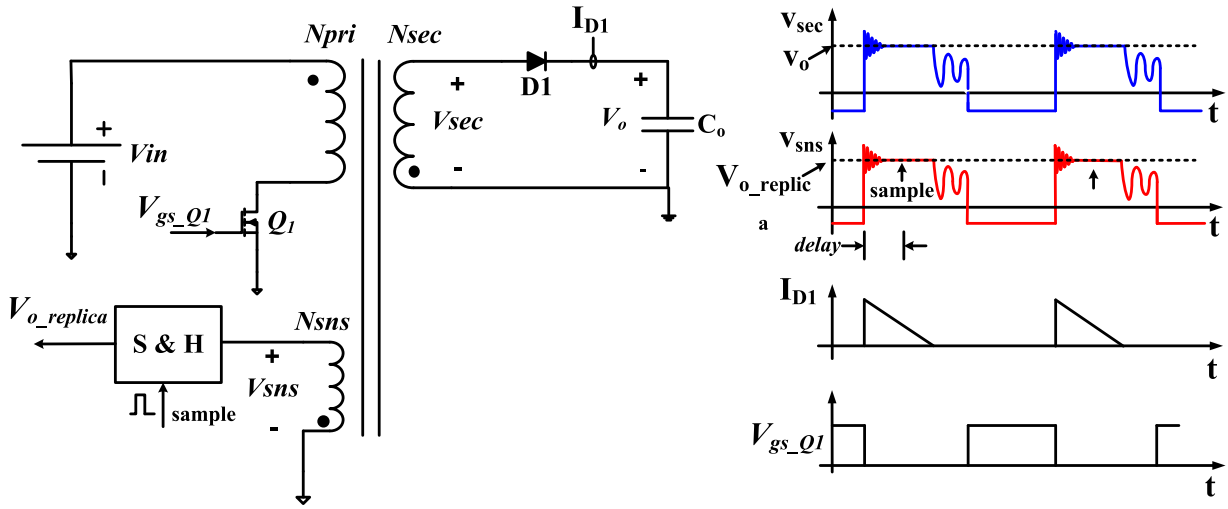


Fig. 11. Primary-side voltage sensing with the flyback topology.

When the output diode is conducting, the voltage on the sensing winding is a valid representation of the output voltage. For the PFC flyback, the output diode does not conduct or conduct a too short period when the input voltage is near zero crossing. Fig. 12 shows the simulated key waveforms and validates this point. The interval *B* is the input voltage zero-crossing region. Both the input voltage and the input current are close to zero. The energy stored in the transformer during the turn on period is very small. During the turn off, the energy is dissipated as conversion loss, and transferred to parasitic capacitors and snubber circuit, before it can force the output diode to conduct or conduct enough time. Valid information from the secondary-side output cannot be extracted at the primary-side during the time interval *B*. On the other side, when the input voltage and the input current are away from the zero crossing in the interval *A*, the output diode conducts for long enough time and provides the time margin to achieve proper voltage sampling.

A solution to solve the aforementioned problem is provided in this paper. The primary-side voltage sensing circuit is modified, as shown in Fig. 13. A DRC network, which included the diode D_e, the resistor R_e, and the capacitor C_e, is added to the output of the S & H circuit.

The operating principle of the circuit is simple and straightforward. As shown in Fig. 13(a), during the time interval $[t_0 - t_1]$, V_{o_replica} (blue line), is a proper representation of the secondary-side output voltage. V_{o_replica} simply passes through the DRC network and is equal to the final sensing output, V_{o_replica1}, with neglecting the diode D_e's forward voltage drop. If somehow a perturbation causes V_{o_replica1} to be higher than V_{o_replica}, the diode D_e is then reversely biased. C_e is discharged through resistor R_e, and the difference between V_{o_replica1} and V_{o_replica} will be reduced and eventually be equal.

During the time interval $[t_1 - t_2]$, the voltage on the sensing winding is not a valid representation of the output voltage during the turn off period. As a result, the sampled voltage is not correct. During this time interval, the diode D_e is reversely biased and V_{o_replica1} is blocked from V_{o_replica}. The resistor R_e discharges

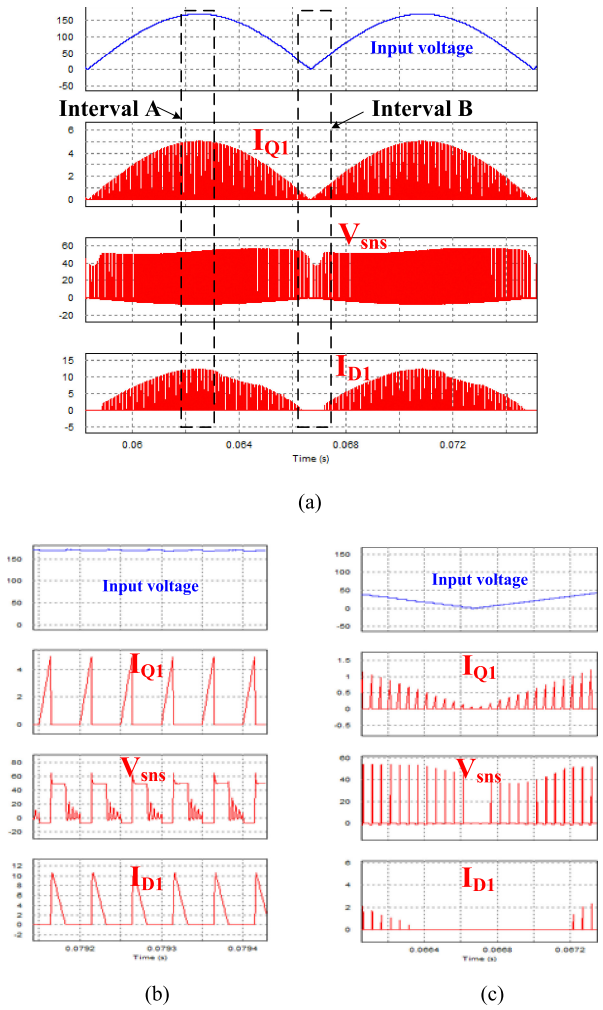


Fig. 12. Simulated key waveforms illustrate the issue of primary-side voltage sensing with the PFC flyback: (a) waveforms in half line cycle time scale, (b) zoom in on interval *A*, and (c) zoom in on interval *B* (simulated with PSIM 9.13).

the capacitor C_e at this period. Similarly, the PFC Flyback main output capacitor Co1 is also discharged by the LED load during this time interval. Therefore, by carefully selecting the resistor R_e and capacitor C_e, the PFC flyback output voltage can be emulated during $[t_1 - t_2]$.

Assuming the turn's ratio between the secondary-side winding and the sensing winding $N_{\rm sec1}$:$N_{\rm sns1}$ is 1:1, C_e and R_e should be selected to meet the following requirement:

$$C_e R_e = C_{o1} R_{\rm LED} \tag{26}$$

where

$$R_{\rm LED} = \frac{V_{o1}}{I_{\rm LED}}. \tag{27}$$

In (26), $V_{\rm o1}$ is the PFC flyback output and $C_{\rm o1}$ is the output capacitor. For example, if the PFC flyback output voltage is 50 V and the LED current is 0.6 A, $R_{\rm LED}$ is equal to 83.3 Ω. When the PFC flyback output capacitor is 470 μF and the calculated equivalent load resistor is 83.3 Ω, C_e and R_e can be designed to be 470 nF and 83.3 kΩ, respectively, to match. When the LED driver is designed to operate under different loading currents, the resistor can also be replaced by a current source that meets the following relationship:

$$\frac{C_e}{I_e} = \frac{C_{o1}}{I_{\rm LED}} \tag{28}$$

where I_e is the current source that emulates the output LED current. The circuit to generate I_e is shown in Fig. 13(c). The current I_e can be calculated as

$$I_e = \frac{V_{\rm ie\_ref}}{R} \tag{29}$$

where $V_{\rm ie\_ref}$ is the emulation current programming voltage. In the LED driver, there is also a voltage, namely, $V_{\rm ILED\_ref}$, to program the LED current. Therefore, as long as the voltage $V_{\rm ie\_ref}$ changes proportionally with the voltage $V_{\rm ILED\_ref}$, the generated emulation current can also change proportional with the load LED current and the emulator can work under different load condition.

By adding a diode, a resistor/current source, and a capacitor to complement the function of the original S & H circuit, the secondary-side output voltage of the PFC flyback can be accurately sensed at the primary side.

C. RCC Flyback Voltage Regulation

Fig. 14 illustrates how the RCC voltage regulation is achieved. As mentioned previously, the PFC flyback output and the RCC output are sensed across the isolation barrier at the primary side. $V_{\rm o1\_replica1}$ is the sensed PFC flyback output (from Fig. 13). First, the dc component of the $V_{\rm o1\_replica1}$ is removed by the dc blocking capacitor C_b. Then the ripple voltage is properly scaled by the ratio of R1 and R2 and added with a dc biasing voltage $V_{\rm bias}$. The result, $V_{\rm o2\_ref}$, is the reference voltage of the RCC output $V_{\rm o2}$. With a well-designed feedback loop, $V_{\rm o2}$ will closely follow its reference voltage. Therefore, V_{o2} contains an opposite twice-line-frequency ripple voltage to that of V_{o1}. Ripple cancellation between the PFC flyback output and the RCC flyback output can be achieved.

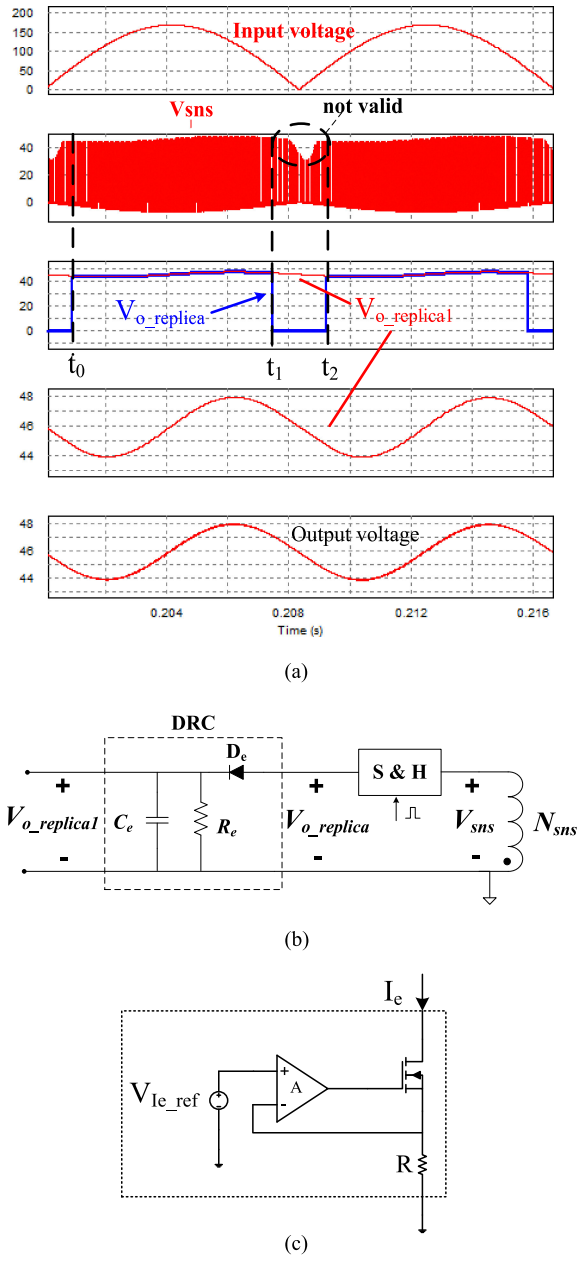


Fig. 13. Improved primary-side voltage sensing: (a) simulated waveforms (simulated with PSIM 9.13), (b) improved voltage sensing circuit, and (c) current source circuit.

D. Primary-Side Current Sensing Strategy

Fig. 2 illustrates the operating principle of the primary-side current sensing. When a flyback converter works under DCM or BCM, by sensing the peak switching current at the primary side $I_{\rm pri\_pk}$ and the transformer current discharge time during turn off $T_{\rm dis}$, the averaged output current $I_{\rm sec\_avg}$ in a switching cycle can be calculated as

$$I_{\rm sec\_avg} = \frac{I_{\rm pri\_pk} \times T_{\rm dis} \times N_{\rm pri}}{2 \times T_s \times N_{\rm Sec}} \tag{30}$$

where T_s, $N_{\rm pri}$, and $N_{\rm sec}$ are the switching period, the primary-side turns, and the secondary-side turns, respectively. T_s, $N_{\rm pri}$, and $N_{\rm sec}$ are the known parameters in the design. A proper

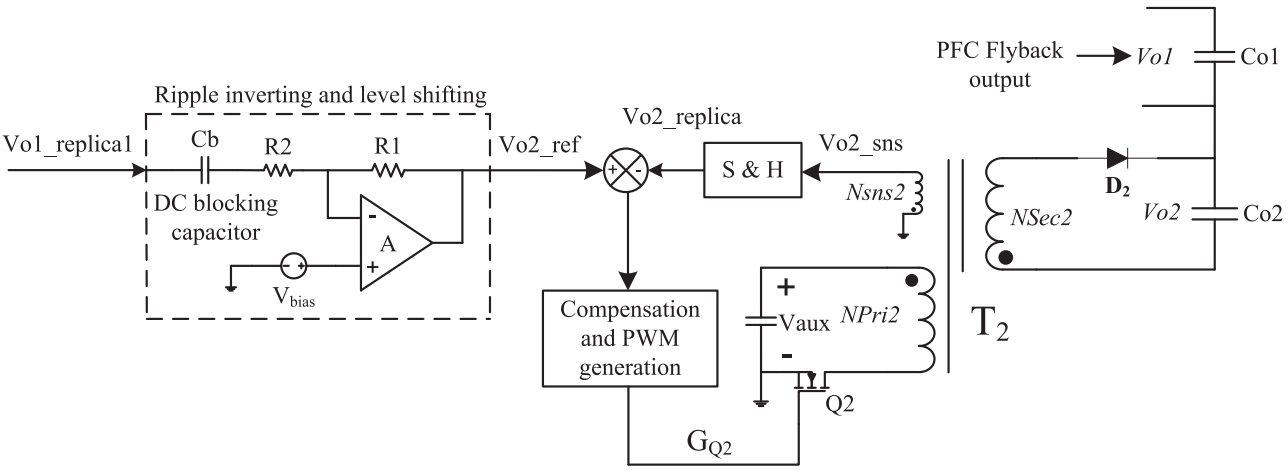


Fig. 14. RCC flyback output regulation loop.

circuit built at the primary side can be used to present the calculation in (30). Therefore, the averaged secondary-side current, which is also the averaged LED current, can be obtained at the primary side.

As shown in Fig. 5, the PFC flyback has one main output $V_{\rm o1}$, located at the secondary side, and another auxiliary output $V_{\rm aux}$, located at the primary side. $V_{\rm aux}$ is also the input voltage of the RCC flyback. For the PFC flyback transformer, there are magnetic current flowing in both the secondary-side winding $N_{\rm sec1}$ and the primary-side auxiliary winding $N_{\rm aux}$ during turn off period. Therefore, the peak switching current at the primary side of the PFC flyback transformer is not an accurate representation of the peak current at the secondary side. Thus, (30) is not applicable to calculate the averaged secondary-side current in the PFC flyback transformer. On the other hand, the RCC flyback has only one output. The peak switching current at the primary side of the RCC flyback transformer is an accurate representation of the peak switching current at the secondary side, and (30) can be used to calculate the averaged secondary-side current. Because the output V_{o2} is connected in series with the LED load, the averaged secondary-side current of the RCC flyback is equal to the averaged LED current. Therefore, in the proposed LED driver, the LED current is sensed at the primary side of the RCC flyback.

E. Accurate LED Current Calculation

With the peak switching current $I_{\rm pri\_pk}$ and the secondary-side current discharging time $T_{\rm dis}$ being sensed, the averaged LED current can be calculated at the primary side. Fig. 15 shows the circuit implementation used in the proposed LED driver.

The primary-side current $I_{\rm pri}$ from the RCC flyback transformer is converted to the voltage form $V(\rm I_{pri})$. The peak of $V(\rm I_{pri})$ is sampled at the end of the turn on period by the S & H circuit. The S & H circuit can also be implemented with a circuit consisting of a diode, a capacitor, and a resistor in order to reduce cost. $V(I_{\rm pri})$ represents the peak primary-side switching current and also the peak secondary-side switching current as the turn's ratio is known. The MOSFET Q_{a1} and Q_{a2} are operated in the complementary fashion. Q_{a1} is turned

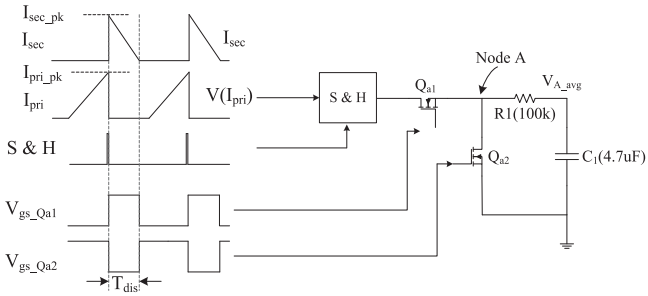


Fig. 15. Primary-side current calculating circuit.

ON when $V(I_{\rm pri})$ is sampled and is turned OFF when the inductor current is discharged to zero. Therefore, the average voltage on the switching node *A* can be expressed as

$$V_{A\_\rm avg} = \frac{V(I_{\rm pri}) \times T_{\rm dis}}{T_S} \tag{31}$$

where $T_{\rm dis}$ is the RCC flyback secondary-side current discharge time. Because $V(I_{\rm pri})$ represents the peak secondary-side switching current, and by comparing (30) and (31), it can be concluded that $V_{A\_\rm avg}$ is a proportional representative of the averaged secondary-side/LED current. The resistor R1 (100 kΩ) and the capacitor C1 (4.7 μF) smooth the waveform to dc.

F. LED Current Regulation

The averaged LED current $I_{\rm avg}$ is measured at the primary side with the circuit shown in Fig. 15. $I_{\rm avg}$ is regulated by the current loop and always follows the current reference $I_{\rm ref}$. The PFC controller is in the LED current feedback loop and adjusts the flyback output voltage. The PFC flyback output voltage settles to the value where the LED current is equal to the current reference. It should be noted that in the proposed LED driver, the dc voltage of the RCC flyback output is a constant in the design and is not in the LED current loop. A wide range of output LED voltage and current can be provided by adjusting the PFC flyback output voltage while keeping the RCC flyback output voltage small for high efficiency.

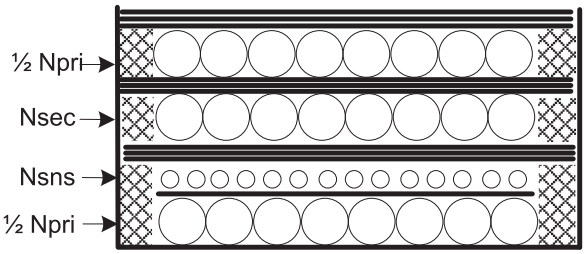


Fig. 16. Recommended transformer construction.

G. Transformer Design

A split primary-side winding construction can effectively improve the coupling between the primary side and the secondary side, reducing the leakage inductance. At the same time, in order to sense the output voltage V_{o1} and V_{o2} with high fidelity at the primary side, it is also very critical to achieve good coupling between the sensing windings and the secondary-side windings. The following transformer construction shown in Fig. 16 is recommended. The first half of the primary-side main winding is placed at the most inner layer. With placing the sensing winding at the second layer and the secondary main winding at the third layer, good coupling between the secondary-side main winding and the sensing winding is achieved. Another half of the primary-side main winding is placed at the outmost layer to achieve good coupling between the primary-side main winding and the secondary-side main winding.

H. Practical Operation Considerations

The proposed LED driver can incorporate a series of practical design measures as a conventional LED driver. During the start-up, the controller circuit should be powered by the AC input voltage and ready to operate before enabling the power stage circuit. In this way, the voltage and the current sensing can be properly performed. After the control circuit is ready, the power stage circuit then starts operating. Overload protection can also be included in a practical design. The overload current condition can be sensed at the primary side, and the protection circuits can shut down the PWM controller if the overcurrent condition is active over a predefined time. The LED load open-circuit and short-circuit protection can also be incorporated into the proposed LED driver. The unusual high LED voltage (open circuit) or low LED voltage (short circuit) are reflected on the output V_{o1}. When the sensed V_{o1} voltage is beyond the predefined limit, the controller can shut down the LED driver. With careful design, the proposed LED driver can operate as practical as a conventional LED driver.

V. Experimental Result

In this section, the simulation and experimental results of the 30 W (50V/0.6A) experimental prototype have been shown to validate the proposed primary-side-controlled LED driving solution. Table I shows the key circuit parameter of the experimental prototype.

Fig. 17 shows the primary-side voltage sensing of the PFC flyback output with the original voltage sensing circuit. It is shown that during $[t_1 - t_2]$, the voltage on the sensing winding is not a valid representation of the PFC flyback output, and the sampled output has a significant voltage dip in the same time interval.

Fig. 18 shows the sensed result of the PFC flyback output voltage with the improved primary-side voltage sensing circuit. During the time interval $[t_0 - t_1]$, the primary-side voltage sensing is achieved by sampling the sensing winding voltage. During the time interval $[t_1 - t_2]$, the output voltage is emulated. By comparing the shape of the sensed output and the PFC flyback output, it is clearly demonstrated that the ripple voltage of the PFC flyback output has been properly presented on the primary side.

TABLE I
Key Circuit Parameter of the Experimental Prototype

Overall LED Driver	
Input voltage range	90 to 265 Vrms
Output voltage	Up to 50 Vdc
Output current	Up to 0.6 Adc
PFC Flyback	
Transformer turns ratio N_{pri1}:N_{sec1}	38:15
Primary-side winding inductance (L_{pri})	470 μH
Main MOSFET	STF11NM80 (800 V, 11 A)
Output diode	YG975C6R (600 V, 20 A)
Output capacitor	ELXY630ELL471MK35S(470 μF, 63 V)
Flyback Ripple Cancellation Converter	
Transformer turn's ratio N_{pri2}:N_{sec2}	1:1
Primary-side winding inductance	RM 5 core (20 μH)
Main MOSFETs	SUD50N04-37P-T4-E3 (40 V, 5.4 A)
Output diode	SSA33L-E3/61T (30 V, 3 A)
RCC input capacitor	UPW1C151MED (150 μF, 16 V)
RCC output capacitor	C2012X5R1C226M125AC (22 μF, 16 V)
Primary-Side Controller	
S & H amplifier	HA5351IBZ
OpAmp	TLV274
PFC flyback controller	FA5601N
RCC flyback controller	FAN6961
LED Load Section	
LED load	23 LEDs connect in series to produce 50 V LED load PN: LR W5AM-HZJZ-1-Z

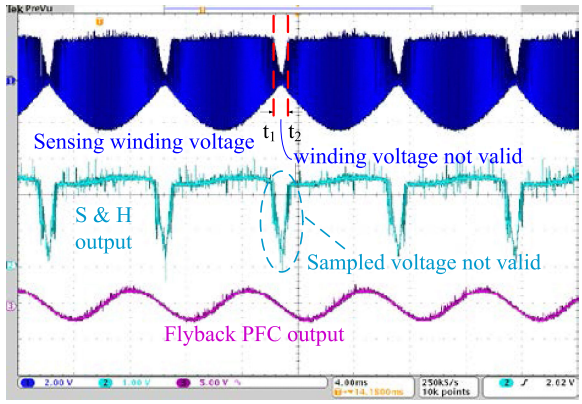


Fig. 17. Primary-side PFC flyback output voltage sensing with the original voltage sensing circuit (under 110 Vrms input voltage).

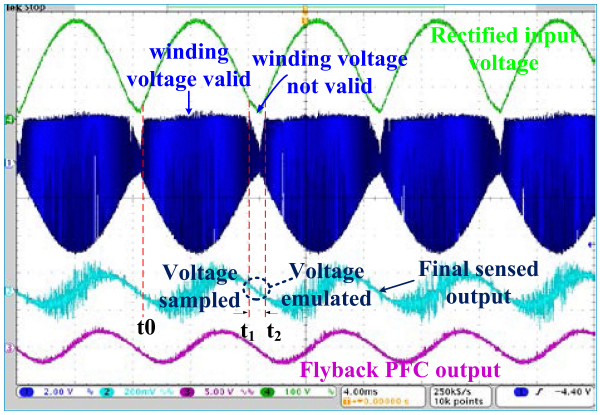


Fig. 18. Primary-side PFC flyback output voltage sensing with the improved voltage sensing circuit (under 110 Vrms input voltage).

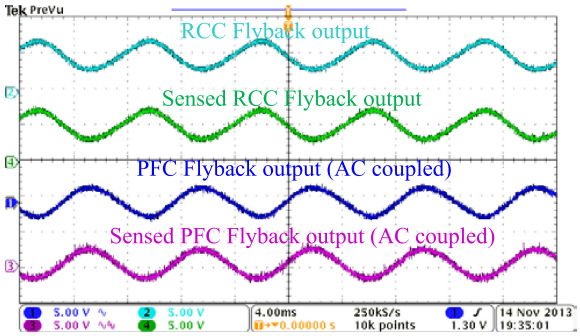
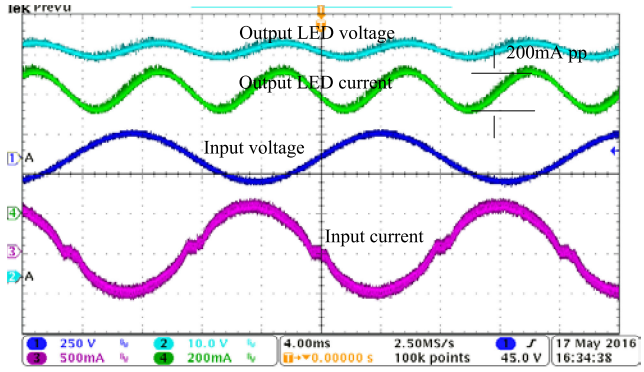


Fig. 19. Ripple cancellation between the PFC flyback output and the RCC flyback output (under 110 Vrms input voltage).

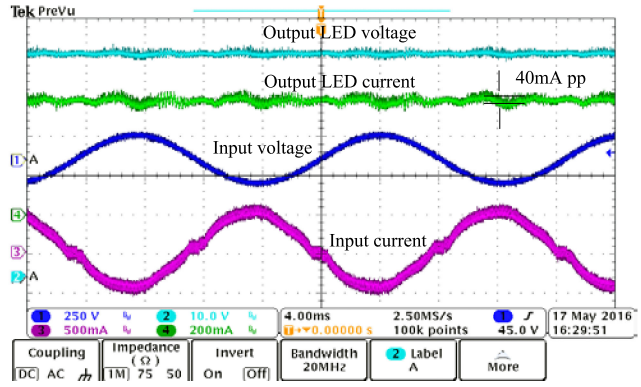
Because the voltage scale is 200 mV/div for the sensed output voltage, the signal level is quite small and, therefore, the noise picked up by the measurement equipment becomes very obvious. When the noise in the sensed output voltage is removed, the sensed output voltage becomes quite clean, as shown in Fig. 19.

The waveforms of ripple voltage cancellation between the PFC flyback and the RCC flyback are shown in Fig. 19. An opposite ripple voltage is generated by the RCC flyback and is used to cancel the twice-line-frequency ripple voltage from the PFC flyback.

The ripple current performance between the proposed primary-side-controlled LED driver and a comparable conventional flyback LED driver is shown in Fig. 20. The same 470 μF output storage capacitors are used in both designs. Under the same averaged 600 mA output current, the low-frequency ripple current with the conventional LED driver goes to 200 mA peak to peak (16.6% ripple current) while the low-frequency ripple current with the proposed LED driver is around 40 mA peak to peak (3.32% ripple current). The low-frequency ripple current has been reduced by five times with the proposed primary-side-controlled ripple cancellation LED driver. The ripple cancellations result can be further improved when the voltage feedback loop of the RCC is optimized and can achieve comparable low ripple performance as a two-stage design.



(a)



(b)

Fig. 20. Low-frequency ripple current performance comparison. (a) The conventional flyback LED driver. (b) The proposed LED driver (under 110 Vrms input voltage, 30 W, 50 V/0.6 A output).

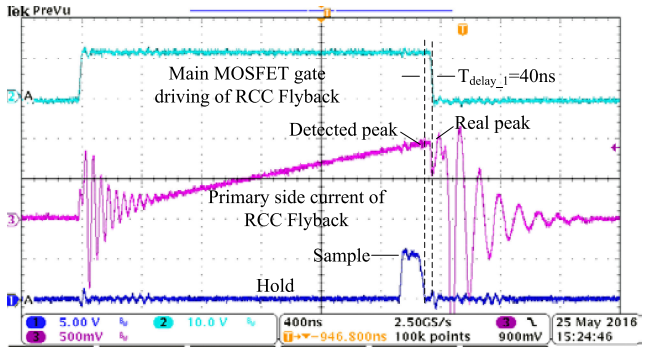


Fig. 21. Primary-side switching current sampling of the RCC flyback.

Fig. 21 shows the primary-side current sampling waveform of the proposed LED driver. The peak primary-side switching current of the RCC flyback is sampled in every switching cycle. In a real circuit implementation, there is a time delay, $T_{\text{delay\_1}}$ between the falling edge of the hold signal and the falling edge of gate driving signal. As a result, there is a small discrepancy between the detected peak switching current and the real peak switching current. The accuracy of the switching current sampling can be achieved with an optimized circuit design. Fig. 22 shows the sampled result of the peak primary-side switching current.

Fig. 23 shows the waveforms that illustrate the calculation of the LED current corresponding to Fig. 15. The turn on time

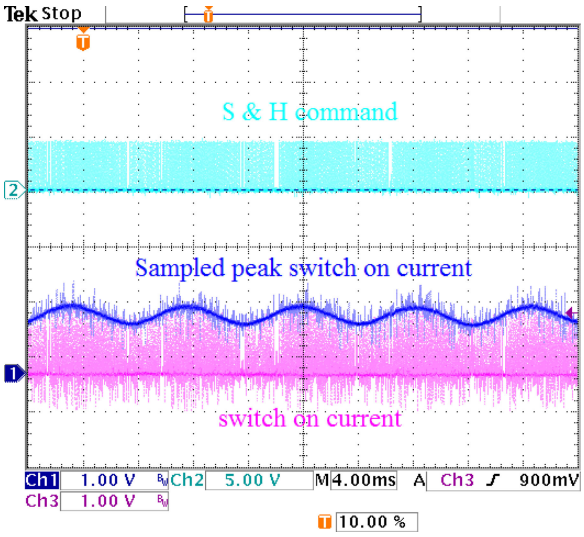


Fig. 22. Sampled primary-side peak switching current.

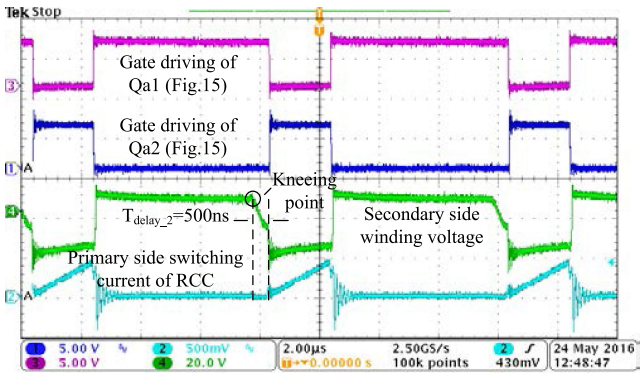


Fig. 23. Key waveforms used in LED current calculation.

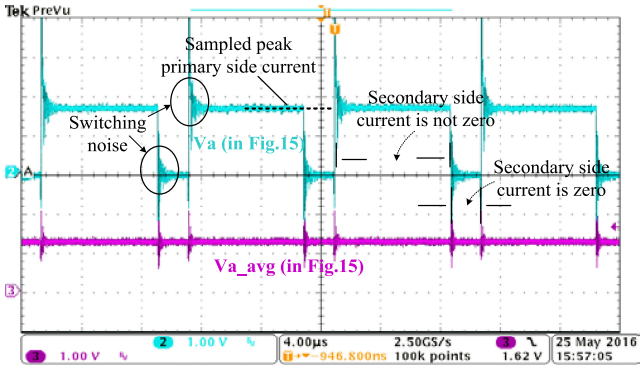


Fig. 24. Primary-side current sensing result.

of Q_{a1} represents the secondary-side current conducting time of the RCC in one switching cycle while the turn on time of Q_{a2} represents the primary-side current conducting time. The voltage on the secondary-side winding serves to detect zero-current conduction. The secondary-side voltage is clamped to be equal to the output voltage until the secondary-side current becomes zero. The kneeing point represents the actual time that the secondary-side current becomes zero. The experimental

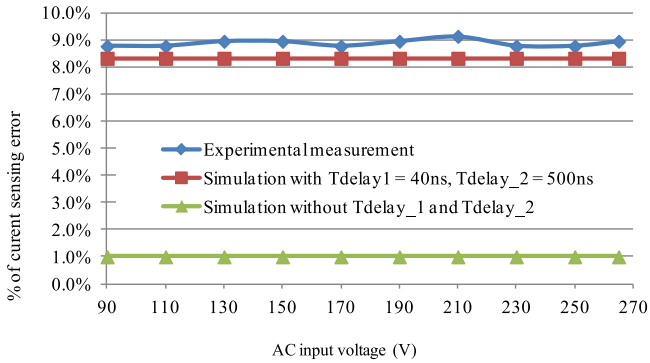


Fig. 25. Primary-side current sensing error under 30 W, 50 V/0.6 A output.

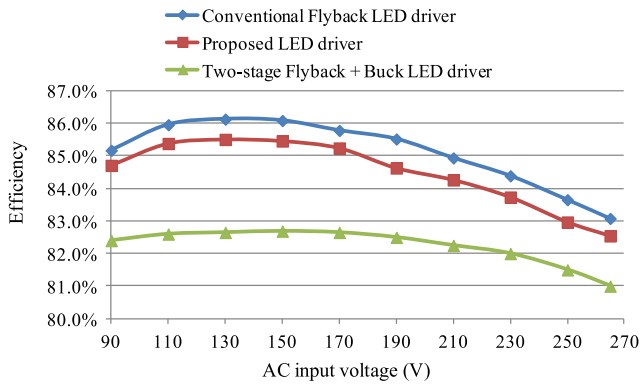


Fig. 26. Efficiency comparison between three different designs under 30 W, 50 V/0.6 A output.

prototype uses the built-in function from FAN6961 to detect the zero-current condition. There is another delay, $T_{\mathrm{delay\_2}}$ between the secondary side current goes to zero and when it is detected. It shows in Fig. 23 that the delay time is around 500 ns, and it is the most significant source that affects the accuracy of sensing the LED current. With a more sophisticated detecting circuit, the kneeing point can be detected that will significantly minimize the time delay $T_{\mathrm{delay\_2}}$.

Fig. 24 shows the LED current sensing results corresponding to Fig. 15. V_a represents the voltage at the switching node, and V_{a_avg} represents the averaged voltage of V_a. V_{a_avg} is the proportional representation of the LED current and is used in the feedback circuit to achieve LED current regulation. In a real design, the noises at the switching node should be minimized in order to reduce the primary-side current-sensing error.

The blue curve in Fig. 25 shows the percentage of primary-side current sensing error of the experimental prototype LED drive under full load. Due to the aforementioned nonideal circuit behavior, such as the error of peak current detection and the error of the secondary-side current conducting time and the switching noise, the primary-side current sensing result is deviated around $+9\%$ from the measured LED current under the full-load condition. Because the RCC operation is quite independent of the ac input voltage, the error is very constant over the entire ac input voltage range. The red curve shows the simulation result with delay time $T_{\mathrm{delay\_1}} = 40$ ns and $T_{\mathrm{delay\_2}} = 500$ ns. The

TABLE II
COMPONENTS OF THE SECOND-STAGE DC–DC AND THE FLYBACK RCC

Components	Second-Stage DC/DC	Flyback RCC
MOSFET	100 V, 5 A such as ZXMN10A09KTC	SUD50N04-37P-T4-E3 (40 V, 5.4 A)
Diode	100 V, 5 A such as SK510L-TP	SSA33L-E3/61T (30 V, 3 A)
Gate driver	High-side and low-side gate driver such as FA5650	None
PWM controller	Such as UC2843	FAN6961
Inductor /Flyback transformer	RCP1317NP-470MMT, 47 μH, 69 mΩ, 13.5 mm diameter, 17.5 mm (high)	RM5 core (20 µH)
Buck output capacitor	470 µF, 63 V electrolytic	20 µF/16 V ceramic

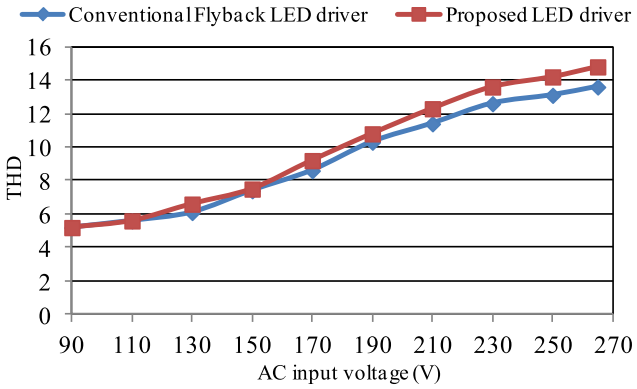


Fig. 27. THD comparison between the proposed LED driver and the conventional flyback LED driver under 30 W, 50 V/0.6 A output.

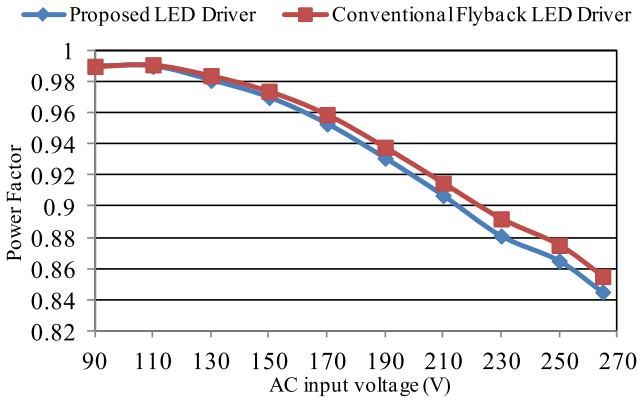


Fig. 28. Power factor comparison between the proposed LED driver and the conventional flyback LED driver under 30 W, 50 V/0.6 A output.

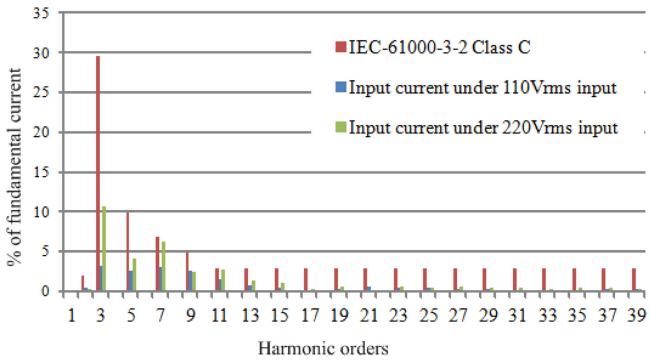


Fig. 29. Input current harmonics measurement.

noise contribution to the primary-side current sensing error is not added to the simulation. The simulated LED current sensing error is deviated 8.3% from the actual LED current, which is fairly close to the experiment result. The green curve shows the simulation result when both $T_{\mathrm{delay\_1}}$ and $T_{\mathrm{delay\_2}}$ are removed. The simulated LED current sensing error is within 1% of the actual LED current. The focus of this paper is to demonstrate an LED driving solution that combines the advantages of both primary-side control and ripple cancellation LED driving. The optimization of the primary-side current sensing circuit is not the objective of the paper. Comparing the experimental and simulation results, we can conclude that the primary-side current sensing method works properly with the proposed power topology and accurate primary-side current sensing can be achieved with an optimized current sensing circuit.

Fig. 26 compares the efficiency of three different designs: the conventional single-stage flyback LED driver, the proposed LED driver, and the two-stage (PFC flyback + buck dc–dc) LED driver. The input power is measured with the built-in function of the ac input source. The LED current and the LED voltage are measured with multimeters to obtain the output power. The PFC flyback converters used in three designs are identical. The components comparison between the second-stage dc–dc converter of the two-stage LED driver and the RCC of the proposed LED driver is shown in Table II. Since the flyback RCC only process a small portion (less than 10%), the power components used in the RCC flyback can have much lower voltage and current rating than the components in the second-stage dc–dc. In this comparison the buck dc–dc converter in the two-stage design achieved a 96.5% efficiency, while the RCC flyback used in the proposed design achieves around 87.5% efficiency. Since the RCC flyback only processes a very small portion of the total output power, the efficiency of the RCC flyback does not have too much impact on the overall efficiency. Therefore, although the second-stage dc–dc converter has much higher efficiency than the RCC flyback, the overall efficiency of the proposed primary-side-controlled ripple cancellation LED driver is still much higher than the two-stage design. It is observed in the experimental that the proposed LED driver achieves around 2.5% higher efficiency than the conventional two-stage LED driver. The advantages of the proposed power topology enable a much higher efficiency design.

It is noted that the efficiency of the conventional flyback LED driver serves as the benchmark for the comparison. In the experimental prototype, the maximum current stress of the MOSFET and diode from the PFC flyback are around 2 and 5 A, respectively. We selected the current rating of the devices

four to five times higher (as shown in Table I) to provide a good margin for thermal and transient considerations. In a practical design, the current rating of the MOSFET and the diode can be reduced to save cost. The efficiency of three designs might be a bit lower than the curves shown in Fig. 26 when lower current rated devices are used. However, the comparison is still fair and valid since the PFCs are the same in three different designs.

The total harmonic distortion (THD) and the power factor performance of the proposed LED driver have been presented in Figs. 27 and 28. The proposed LED driver achieved a comparable power factor and THD performance as a conventional Flyback LED driver.

Each order of input current harmonics had also been measured, and the result is shown in Fig. 29. The measured harmonic currents are within the limit required by IEC-61000-3-2 Class C under both 110 and 220 Vrms input voltage.

VI. Conclusion

A primary-side-controlled ripple cancellation LED driver has been proposed in this paper. The power stage is constructed by a PFC flyback and a flyback RCC. The RCC flyback is used to generate an opposite twice-line-frequency ripple voltage to that of the PFC flyback output. Ripple cancellation is achieved by connecting the output voltage of the RCC flyback and the output voltage of the PFC flyback in series. As the result, a dc LED voltage is produced and is used to drive the LED load with a dc LED current. The primary-side control is achieved by sensing the PFC flyback output voltage, the RCC flyback output voltage, and the LED current at the primary side and building the entire control circuit at the primary side. The design guideline on how to select a component is also provided. A universal input 30 W (50 V, 0.6 A) output experimental prototype has been built to verify the proposed LED driver. It achieved 3.32% peak-to-peak twice-line-frequency ripple LED current (flicker-free), 85.5% full-load efficiency, and 0.99 PF.

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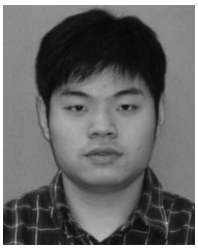
Peng Fang (S'11) received the M.Sc. degree from Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong, in 2007. He is currently working toward the Ph.D. degree in electrical engineering at Queen's University, Canada.

From 2008 to 2011, he worked at ASM Pacific Technology as an R&D Power Electronics Engineer, where he lead the innovation and development on switching mode power supply, switching and linear power amplifier. He has two U.S. patents pending and several inventions. His research interests include LED driver, power factor correction, PV inverter, resonant converter, and energy harvesting technologies.

Mr. Fang won the second place in the IEEE Kingston section Research Excellent Award.



Ya-jie Qiu (S'13) received the M.Sc. degree from Anhui University of Technology, Huainan, China, in 2011. He is currently working toward the Ph.D. degree in electrical engineering at Queen's University, Kingston, ON, Canada.

His current research interests include topologies and control methods for ac–dc converters with power factor correction and LED driver, nonlinear control to achieve fast dynamic performance for dc–dc converters, and modulation schemes for resonant converters. He has two U.S. patents pending.

Mr. Qiu won the outstanding presentation award at APEC'15 and a conference travel award from PSMA.

Hongliang Wang (M'12–SM'15) received the B.Sc. degree from Anhui University of Science and Technology, Huainan, China, in 2004, and received the Ph.D. degree from Huazhong University of Science and Technology, Wuhan, China, in 2011.

From 2004 to 2005, he worked as an Electrical Engineer of Zhejiang Hengdian Thermal Power Plant. From 2011 to 2013, he worked as a Senior System Engineer of Sungrow Power Supply Co., Ltd. Since 2013, he has been a Postdoctoral Fellow at Queen's University, Kingston, ON, Canada. His research interests include the area of power electronics, including digital control, modulation and multilevel topology of inverter for photovoltaic application and micro-grids application; parallel technology and Virtual Synchronous Generator (VSG) technology; and dead time compensation, filter optimization and Common mode voltage elimination; resonant converters and server power supplies, and LED drivers. He has published more than 40 papers in conferences and journals. He is the inventor/co-inventor of 39 China issued patents, 11 U.S. pending patents, and 4 PCT pending patents.

Dr. Wang is currently a Senior Member of China Electro-Technical Society; a Senior Member of China Power Supply Society. He serves as a Member of CPSS Technical Committee on Standardization; a Member of CPSS Technical Committee on Renewable Energy Power Conversion; the Vice-Chair of Kingston Section, IEEE; a Session Chair of ECCE 2015; a TPC Member of ICEMS2012; and a China Expert Group Member of IEC standard TC8/PT 62786.

Yan-Fei Liu (M'94–SM'97–F'13) received the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 1994.

From February 1994 to July 1999, he was a Technical Advisor with the Advanced Power System Division of Nortel Networks. Since 1999, he has been with Queen's University, Kingston, ON, Canada, where he is currently a Professor in the Department of Electrical and Computer Engineering. His current research interests include digital control technologies for high efficiency, fast-dynamic-response dc–dc switching converter, ac–dc converter with power factor correction, resonant converters and server power supplies, and LED drivers. He holds 20 U.S. patents and has authored or coauthored more than 190 technical papers in the IEEE transactions and conferences.

Dr. Liu is a Principal Contributor for two IEEE standards. He has been an Editor of the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS OF POWER ELECTRONICS (IEEE JESTPE) since 2012 and an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2001. He was an Editor-in-Chief for the special issue of Power Supply on Chip of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2011 to 2013. He was the ECCE 2015 General Co-Chair in charge of technical program. He will serve as the ECCE 2019 General Chair. In addition, he has been the Chair of the PELS Technical Committee on Control and Modeling Core Technologies since 2013. He was the Chair of the PELS Technical Committee on Power Conversion Systems and Components from 2009 to 2012.